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4.1 Soldering Heat Resistance

As electronic equipment products become more compact and multi-function, Surface Mount Devices (SMD) have become widely used in recent years, and the trend is towards greater numbers of pins and larger packages. One kind of trouble that must be kept in mind when handling SMD is package cracking that can occur when soldering is performed using a reflow oven or other method that heats the entire package.

To prevent this problem, the Sony Semiconductor Business Unit improves package materials and structures, ranks each product according to the package cracking resistance (hereafter “SMD code”), and requests that customers perform solder mounting based on these ranks.

This section describes the package cracking mechanism, SMD code, and other notes to prevent package cracking in the mounting process. Notes on soldering for all semiconductor products are described in section 4.4.

4.1.1 Generation Mechanism

(1) Package cracking phenomena

Package cracking during mounting occurs through the following process. (See Fig. 4-1.)

![Fig. 4-1 Package Cracking Phenomena](image)

① When the moisture-proof packing is opened and an SMD is exposed to ambient conditions during storage or the mounting process, the moisture in the air adsorbs to the surface of the resin that forms the package and diffuses to the inside of the package. This diffusion progresses over time, and the moisture...
reaches the boundary between the chip or die pad and the resin inside the package.

2. When soldering is performed by reflow or another method that heats the entire package in the condition in 1 above, the entire SMD is exposed to high temperature, causing moisture present at the boundary to gasify and expand. As a result, the water vapor pressure inside the minute gaps at the boundary rises rapidly, causing stress to concentrate at the edges of the chip or die pad. When this stress exceeds the thermal strength of the resin, package cracking occurs.

3. Trouble that occurs due to cracking differs according to the cracking location.

When cracking occurs on the chip side, the wires that provide electrical conductivity between the chip and the leads may be severed, or the boundary between the resin and the chip may delaminate, causing the humidity resistance to deteriorate. When cracking occurs on the die pad side, the package expands during solder melting, which may result in a soldering defect.

(2) Factors causing package cracking: Boundary moisture density

As described above, moisture absorption in the package is a major factor causing package cracking. However, in precise terms it is not the absolute sum total of the moisture absorbed that is the problem, but the moisture density at the boundary between the chip or die pad and the resin inside the package that is the factor causing package cracking.

The course of moisture absorption and derivation of the boundary moisture density are described below. (See Fig. 4-1.)

Generally, when solid materials are exposed to air, water molecules are adsorbed to the surface mainly by the van der Waals interaction. The organic materials used in SMD packages are thought to have stronger affinity to water molecules compared to inorganic materials.

The moisture density $Q_s$ adsorbed to the package surface is expressed by the following equation in accordance with Henry’s Law as a function of the inherent solubility coefficient $S$ of the materials and the atmospheric water pressure $P_a$.

$$Q_s = S \cdot P_a \quad \cdot \cdot \cdot \text{Equation 4.1.1}$$

Here, the solubility coefficient $S$ can be expressed by the following equation as a function of the activation energy $E_s$ and temperature $T$.

$$S = S_0 \exp(E_s/kT) \quad \cdot \cdot \cdot \text{Equation 4.1.2}$$

$k$: Boltzmann constant, $S_0$: Constant

The moisture adsorbed to the package moves to the inside of the package by the diffusion phenomenon; that is to say, until the density gradient disappears. At this time, moisture is constantly supplied from the air to the
package surface and the moisture density determined by Equation 4.1.1 is maintained. The diffusion phenomenon follows Fickian diffusion within the environmental temperature range of the SMD storage and mounting processes, and can be expressed by the following equation as a function of the diffusion coefficient D, position coordinate x, and time t.

\[ \frac{\partial Q(x,t)}{\partial t} = D \frac{\partial^2 Q(x,t)}{\partial x^2} \quad \cdots \cdot \cdot \cdot \text{Equation 4.1.3} \]

Here, the diffusion coefficient D can be expressed by the following equation as a function of the activation energy Ed and temperature T.

\[ D = D_0 \exp(Ed/kT) \quad \cdots \cdot \cdot \cdot \text{Equation 4.1.4} \]

k: Boltzmann constant, D0: Constant

This boundary moisture density, which is a factor causing package cracking, can be obtained from Equations 4.1.1 to 4.1.4 above. The Sony Semiconductor Business Unit evaluates resistance to package cracking with the focus on this boundary moisture density, and determines the SMD code described hereafter for each product.

(3) Factors causing package cracking: Package exposure temperature during soldering

As described above, package cracking occurs when moisture that has reached a boundary gasifies and expands rapidly during soldering, causing the internal stress to exceed the thermal strength of the resin that comprises the package. In addition, the probability of occurrence rises together with the package exposure temperature. This is due to the temperature dependence of the water vapor pressure generated inside the gaps at the package boundaries and the strength of the resin that comprises the package.

For example, comparing exposure temperatures of 220°C and 260°C, the temperature dependence of the saturation water vapor pressure shows that at 260°C, the water vapor pressure rises by approximately twice as much and the resin strength falls to approximately half compared to 220°C. (See Fig. 4-2 and Fig. 4-3.)
(4) Factors causing package cracking: Package structure and materials

Even when SMD are exposed to the same ambient conditions for the same time before soldering, the boundary moisture density that is an occurrence factor exhibits different values due to differences in the thickness, solubility coefficient and diffusion coefficient of the resin over the semiconductor chip or under the die pad that acts as the diffusion path.

In addition, the stress $\sigma$ generated inside the solder is expressed by the following equation based on a fixed-edge uniform load model. Here, $a$ is the short edge of the chip or die pad, $k$ is a coefficient determined by the ratio between the short edge $a$ and the long edge $b$, $h$ is the thickness of the resin over the chip or under the die pad, and $P$ is the water vapor pressure inside the package. (See Fig. 4-4.)

$$\sigma = 6k \frac{a}{h} P$$  \hspace{1cm} \text{Equation 4.1.5}

This means that even when the boundary moisture density and the solder exposure temperature that is another occurrence factor are the same, the cracking occurrence rate differs due to differences in the semiconductor chip or die pad size.

![Fig. 4-4 Fixed Edge Uniform Load Model](image-url)
4.1.2 Surface Mount Device Code

The Sony Semiconductor Business Unit expresses the solder heat resistance for SMD reflow and solder dipping using a four to eight character SMD code. This code indicates the allowable shelf time and allowable number of soldering times for SMD exposed to ambient conditions of 30°C and 70%RH after the moisture-proof packing is opened until soldering.

There are 20 different SMD codes as shown in Table 4-1.

<table>
<thead>
<tr>
<th>No.</th>
<th>SMD code</th>
<th>No.</th>
<th>SMD code</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R390F390</td>
<td>11</td>
<td>R304F390</td>
</tr>
<tr>
<td>2</td>
<td>R390F308</td>
<td>12</td>
<td>R304F308</td>
</tr>
<tr>
<td>3</td>
<td>R390F304</td>
<td>13</td>
<td>R304F304</td>
</tr>
<tr>
<td>4</td>
<td>R390F302</td>
<td>14</td>
<td>R304F302</td>
</tr>
<tr>
<td>5</td>
<td>R390</td>
<td>15</td>
<td>R304</td>
</tr>
<tr>
<td>6</td>
<td>R308F390</td>
<td>16</td>
<td>R302F390</td>
</tr>
<tr>
<td>7</td>
<td>R308F308</td>
<td>17</td>
<td>R302F308</td>
</tr>
<tr>
<td>8</td>
<td>R308F304</td>
<td>18</td>
<td>R302F304</td>
</tr>
<tr>
<td>9</td>
<td>R308F302</td>
<td>19</td>
<td>R302F302</td>
</tr>
<tr>
<td>10</td>
<td>R308</td>
<td>20</td>
<td>R302</td>
</tr>
</tbody>
</table>

Note 1) Reflow conditions: Temperature profile shown in Fig. 4-5.
4.1.3 Notes on Package Cracking

(1) When mounting products, customers are requested to not deviate from the allowable time after opening the moisture-proof packing and allowable number of soldering times specified by the SMD code corresponding to the product, and the SMD exposure atmosphere after opening the moisture-proof packing and soldering temperature conditions that are prerequisites for the SMD code.

(2) When the allowable time after opening the moisture-proof packing is exceeded, products can be used by baking to remove moisture. However, the baking conditions that reduce the boundary moisture density to an appropriate value vary according to the package, so consult your Sony sales representative beforehand when baking is necessary.

(3) When the moisture-proof packing has been opened but products were not mounted, store under conditions of 30°C and 30%RH or less.

(4) Moisture enters the inside of the moisture-proof packing even through tiny holes, with the result that package cracking may occur even under the conditions recommended by the SMD code. Therefore, sufficient care must be given to the handling of SMD packing.

(5) Minute amounts of moisture permeate the laminate bags of even unopened moisture-proof packing, so long-term storage should be avoided.
<References>


3) Saito and Hirai: Practices in Mechanics of Materials
4.2 Notes on Handling for Electric Breakdown

Semi-conductor device transistor sizes are becoming smaller due to decreasing gate oxide film thickness and miniaturization of wiring. As a result, lower resistance to electrostatic discharge (ESD), overvoltage and overcurrent (electric over stress: EOS), noise and other electrical stress is becoming a serious problem. Even slight voltage fluctuations and noise that were not a problem thus far are becoming increasingly likely to cause device misoperation or breakdown.

This section describes countermeasures to prevent semiconductor devices from misoperating or breaking down due to electrical stress.

4.2.1 Electrostatic (ESD) Breakdown

4.2.1.1 Electrostatic Charge Phenomenon

Electrostatic charge refers to when an electric charge migrates due to contact between two objects, and then remains on the objects when they are separated, causing them to become electrically charged. When there is a surplus of electrons in an object it is negatively charged; when there is a shortage of electrons the object is positively charged.

In terms of general electrical properties, objects can be classified as items that easily acquire electrons and items that easily give electrons.

Table 4-2 shows the Faraday triboelectric series. Here, when a higher item in the triboelectric series contacts or rubs against a lower item, the higher item gives electrons and becomes positively charged, while the lower item acquires electrons and becomes negatively charged.

Table 4-3 shows an example of typical static electricity charge voltages.
The two main mechanisms for generating static electricity that causes the electrostatic discharge phenomenon within processes where semiconductor devices are handled are as follows.

**(1) Charging due to contact and separation (rubbing) between objects**

When two objects contact each other, a charge migrates between the objects at the contacting surfaces. (Fig. 4-6(a))

If the objects are separated in this condition, the surface of each object retains this biased charge condition, and becomes electrostatically charged. (Fig. 4-6(b)-(c)) Triboelectric charging is generally held to be the cause of static electricity, and can be thought of as the condition where this contact and separation occur repeatedly.

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**Table 4-2 Frictional Triboelectric Series Table**

<table>
<thead>
<tr>
<th>Positive (+)</th>
<th>Negative (-)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acetate</td>
<td>Glass</td>
</tr>
<tr>
<td>Nylon</td>
<td>Wool</td>
</tr>
<tr>
<td>Silk</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Polyester</td>
<td>Paper</td>
</tr>
<tr>
<td>Cotton</td>
<td>Steel</td>
</tr>
<tr>
<td>Nickel, copper, silver</td>
<td>Zinc</td>
</tr>
<tr>
<td>Rubber</td>
<td>Acrylic</td>
</tr>
<tr>
<td>Polyurethane foam</td>
<td>PVC (vinyl)</td>
</tr>
<tr>
<td>Teflon</td>
<td></td>
</tr>
</tbody>
</table>

**Table 4-3 Examples of Static Electricity Generation**

<table>
<thead>
<tr>
<th>Static electricity source</th>
<th>Charge voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Relative humidity 10% to 20%</td>
</tr>
<tr>
<td>Walking on carpet</td>
<td>35,000V</td>
</tr>
<tr>
<td>Walking on vinyl tile</td>
<td>12,000V</td>
</tr>
<tr>
<td>Person working at a general workbench</td>
<td>6,000V</td>
</tr>
<tr>
<td>Card case</td>
<td>7,000V</td>
</tr>
<tr>
<td>Plastic bag taken from a workbench</td>
<td>20,000V</td>
</tr>
<tr>
<td>Urethane foam cushion chair</td>
<td>18,000V</td>
</tr>
</tbody>
</table>

---

Fig. 4-6 Mechanism for Generating Charges through the Contact and Separation of Objects
(2) Charges due to induction from charged objects

When a charged object approaches an insulated conductor, the effect of the electric field from the charged object produces a charge bias due to electrostatic induction inside the conductor. In this condition, the conductor is in an inductively charged state. (Fig. 4-7(a)) When inductive charging occurs and the charge becomes uneven, if a part of the conductor contacts a ground (GND) or another conductor, a charge having the same polarity as the charged object that approached moves from the conductor to the GND or the other conductor, and the ESD phenomenon occurs. (Fig. 4-7(b)) Furthermore, if the conductor is then separated from the GND and the charged object is moved away from the conductor, the charge in the conductor that was attracted to the charged object becomes free and exists in surplus inside the conductor, which becomes charged with that polarity. (Fig. 4-7(c)) If a part of the conductor then contacts the ground or another conductor again in this condition, the charge is discharged. (Fig. 4-7(d))

When this charge phenomenon is applied to semiconductor devices, the chip and lead frame are treated as conductors. Simply bringing a charged object close to an insulated semiconductor device generates an inductive charge in the chip, and there is the risk of ESD occurring if the pins are contacted with metal. Also, if the surface of a plastic package becomes charged by rubbing or other contact, the surface may act as a charged object to generate an inductive charge in the chip, thus causing ESD in the same manner by inductive charging.
This type of inductive charging does not occur only in semiconductor devices. The same type of inductive charge is produced in ungrounded metal objects, tweezers or other tools held by an insulated glove or finger sacks, PCB wiring patterns, FPC metal wiring and other objects. These items may cause ESD with respect to semiconductor devices in the mounting process.

In this manner, eliminating charged objects that cause inductive charges in devices is also an important countermeasure within processes in which semiconductor devices are handled.

4.2.1.2 ESD Test Methods

Electrostatic discharge phenomena produced by handling semiconductor devices are classified into a number of models according to the charged object and the discharge mode. The testing methods used to evaluate the resistance of semiconductor devices to electrostatic discharge were devised based on these electrostatic discharge models.

(1) Human Body Model (HBM) 3),4),5)

The human body model (HBM) is a testing method that models the discharge of electrostatic charge accumulated in a charged human body to a semiconductor device. This testing method uses the capacitance of the human body (=100pF) and the contact resistance between the human body and the device (=1500Ω). This testing method has been used for quite some time in the U.S. MIL standard (MIL-STD-883D method3015.7), and is thus widely used as a standard test method in Japan and overseas.

(2) Machine Model (MM) 3),6)

The machine model ESD testing method originated as a human body discharge model based on the worst values for human body capacitance and discharge resistance (200 pF/0 Ω). This testing method was used by domestic semiconductor device manufacturers mainly as a means of discovering circuits that are susceptible to electrostatic breakdown during the device design verification. However, it is known that human body discharge can be verified using the human body model (HBM), and that the machine model (MM) simulates excessive discharge phenomena that almost never occur in an actual process due to excessive inductance component (~750 nH) of the discharge path. For these reasons, the MM has been deleted from the above standard.

(3) Charged Device Model (CDM) 7)~11)

The charged device model (CDM) is a testing method that models the phenomenon where the semiconductor device itself carries a charge and the charge inducted to the device from a charged object near the device is discharged. This model is characteristic in that it reproduces the discharge mechanism in the form closest to the discharge phenomenon occurring in the field, so correlations with the ESD failure modes occurring in processes have also been widely confirmed.

The charged device model testing methods are shown in Fig. 4-8. The charged device model connects a high-
voltage source to the device side and accumulates a charge in the parasitic capacitance formed between a grounded electrode plate and the device. This accumulated charge is then discharged to the GND via a metal discharge rod by closing SW1 that is connected to a device pin. Charging and discharging are repeated for each pin of the test device, and the device withstand voltage is evaluated by ultimately applying stress to all pins.

Fig. 4-8 CDM/FICDM Testing Methods
(4) ESD test standards

ESD testing methods adopted in the current standards are shown in Table 4-4. The HBM and CDM testing models are each used as standards, and the human body model (HBM) tests performed in Japan and overseas are virtually the same. In the Japanese domestic JEITA standard, the charged device model (CDM) employs a testing method that performs charging and discharging by contacting a discharge electrode directly to a device pin. In contrast, the CDM in the U.S. JEDEC standard employs the Field Induce CDM (FICDM) testing method that charges the device by inductive charging from an electrode plate to which high voltage is applied, and performs discharging by contacting a discharge electrode.

Table 4-4 Semiconductor Device ESD Testing Methods

<table>
<thead>
<tr>
<th>ESD model</th>
<th>Test circuit</th>
<th>Test standards</th>
</tr>
</thead>
<tbody>
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<td>Human Body Model (HBM)</td>
<td><img src="image" alt="HBM Circuit Diagram" /></td>
<td>JEITA EIAJ ED-4701/304 (2001)</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="HBM Circuit Diagram" /></td>
<td>JEDEC JESD22-A114F (2007)</td>
</tr>
<tr>
<td>Charged Device Model (CDM)</td>
<td><img src="image" alt="CDM Circuit Diagram" /></td>
<td>JEITA EIAJ ED-4701/305A (2004)</td>
</tr>
<tr>
<td></td>
<td><img src="image" alt="CDM Circuit Diagram" /></td>
<td>JEDEC JESD22-C101E (2008)</td>
</tr>
</tbody>
</table>

4.2.1.3 Failure Mechanisms due to ESD Breakdown

The main ESD breakdown mechanisms for semiconductor devices include the following two phenomena.

(1) Thermal breakdown (junction breakdown, melted wiring)

(2) Insulating film breakdown (gate oxide breakdown, interlayer insulator breakdown)
(1) Thermal breakdown

Thermal breakdown phenomena mainly include junction breakdown and melted Metal/Poly wiring. Junction breakdown can occur at relatively low energy, but melted wiring generally requires high energy, so it is thought to occur more from electric over stress (EOS) phenomena such as surge, soldering iron leaks, etc. than due to ESD.

The junction breakdown phenomenon occurs when an excessive current flowing through the junction causes the temperature to rise locally in the junction and exceed the melting point of silicon (1415°C). The Wunsch & Bell model\(^{12}\) that uses a thermal diffusion equation is most generally used as a model to describe this junction breakdown. This model determines the junction breakdown phenomenon from the applied pulse width and the power density applied to the element.

Thermal breakdown requires relatively high energy, so within the process it is caused by discharge from a charged worker (human body) or discharge of the charge accumulated in a large-capacity capacitor or other mounted component. In the ESD breakdown test, this can be observed as the main breakdown mode of the human body model (HBM).

(2) Insulating film breakdown

Insulating film breakdown is a failure mechanism where the gate oxide film or the interlayer insulator shorts. Insulating film breakdown occurs often in devices with thin gate oxide such as MOS devices, and is the most common ESD breakdown failure mechanism seen within the process. The energy required for breakdown is small, so this phenomenon occurs at lower charge levels than thermal breakdown, and ESD breakdown within a process is thought to occur more due to insulating film breakdown than thermal breakdown.

This insulating film breakdown is known as the main breakdown mechanism of the charged device model (CDM).

4.2.2 Electrostatic Countermeasures

The gate oxide film thickness of MOS transistors manufactured using the latest processes has already been reduced to several nm or less, and the endurance voltage of these oxide films is only several voltage. Semiconductor devices employ countermeasures such as circuits to protect against the entry of external static electricity for each input/output pin to prevent static electricity from being applied to the internal transistors. However, it becomes extremely difficult to protect the internal transistors against external static electricity in excess of several 100 V using only protection circuits.

Furthermore, as device operating speeds increase, the effect of the parasitic impedance of protection circuits on operating speed cannot be ignored, and an increasing number of pins requires the reduction of the size of these protection circuits or elimination of the circuits themselves. It is thought that in the latest process the electrostatic endurance voltage of the devices has already dropped due to device miniaturization and increases in operating
speed.

Against this background, countermeasures for preventing electrostatic breakdown become even more important in processes where semiconductor devices are handled. General knowledge required to protect semiconductor devices from electrostatic breakdown during handling, methods for controlling static electricity within processes, and countermeasures against electrostatic breakdown are described below.

4.2.2.1 Basic Electrostatic Discharge Control Concepts

Basic concepts for electrostatic discharge controls in processes where semiconductor devices are handled are as follows.

(1) Designing processes and facilities that do not generate static electricity

During process design or when investigating the introduction of manufacturing facilities, processes with effective electrostatic discharge controls can be constructed by introducing electrostatic discharge control facilities (grounds, floors, environment, etc.) and building countermeasures for preventing the generation of static electricity by friction or contact into the equipment specifications.

(2) Not bringing items that are easily charged by static electricity into processes

Electrostatic breakdown due to triboelectric charging or inductive charging can be prevented by not bringing packing materials, paper, fixtures, office supplies or other insulated objects that easily generate static electricity into processes except when absolutely necessary.

(3) Quickly leaking static electricity that does occur to prevent electrostatic discharge

Chances for electrostatic discharge (ESD) to semiconductor devices can be reduced by quickly leaking generated static electricity using various methods such as grounding equipment and jigs, controlling resistance values on floors and work surfaces, and neutralizing charges with an ionizer. In addition, charges can be gradually leaked without causing sudden discharge and electrostatic breakdown can be prevented by changing metal parts that contact devices to materials with appropriate resistance values.

(4) Periodically checking electrostatic discharge control conditions and maintaining countermeasure effects

After implementing electrostatic countermeasures, the effects of these countermeasures cannot be maintained unless periodic checks are made and control is performed to ensure that the effects are reliably maintained.

(5) Instilling an awareness of the need for electrostatic discharge controls in workers and process controllers

Electrostatic discharge controls require knowledge and understanding of static electricity on the part of employees and process controllers. Electrostatic protective items can be even more effective at preventing
electrostatic breakdown depending on the awareness of the person using them.

Electrostatic discharge controls are not a problem that can be solved simply by introducing electrostatic protective items. Ensuring thorough and consistent countermeasures and spreading general knowledge of electrostatic discharge control concepts can make process managers and workers aware of the risk of electrostatic breakdown, and are effective means of reducing electrostatic breakdown problems within processes.

4.2.2.2 Approach toward Process Control References

In order to control electrostatic charge levels within processes, it is necessary to determine the charge level to use as the control criteria. This control reference is set based on the ESD withstand voltage of the devices handled in that process. However, what is important in determining a control reference is which testing method should be used to obtain the ESD withstand voltage employed as the process control reference guideline among the electrostatic breakdown testing models for devices described in item 4.2.1.2. Even if control criteria are set based on ESD phenomena that do not occur in the process, actual electrostatic breakdown cannot be effectively prevented.

Fig. 4-9 shows the relationship between charged objects present in processes and electrostatic capacity (earth capacity). Objects causing ESD within processes generally have different electrostatic capacities. For example, the electrostatic capacity of the human body is usually said to be approximately 80 to 200 pF\textsuperscript{13)-16), which is equivalent to the capacitance used by the human body model (HBM). In contrast to this, most items other than workers that may produce ESD with devices such as tweezers and metal parts on chip mounters such as device adsorption jigs and positioning stages have electrostatic capacity of fF to 10 and more pF.\textsuperscript{16) In addition, the electrostatic capacity of most semiconductor devices is also mostly within the range of several pF to several 10 pF. (Table 4-5) When the electrostatic capacitance of charged objects becomes smaller in this manner, the accumulated electrostatic energy is lower even when charged to the same voltage, so semiconductor devices are less likely to experience electrostatic breakdown.
Failures produced by the discharge of static electricity accumulated in small electrostatic capacity clearly differ in most cases from failure modes when static electricity is discharged from the comparatively large capacitances (100, 200 pF) such as HBM or MM tests.\textsuperscript{17)\textendash20}) As seen in Fig. 4-9, the charged device model (CDM) testing method that uses the parasitic capacitance is thought to be the most suitable testing method for reproducing phenomena where static electricity is discharged from small capacitance charged objects within processes.\textsuperscript{18), 20\textendash22})
In this manner, an appropriate charge level control value for charged objects within processes should be set according to the type of charged object. Thus, more realistic charge level control criteria can be set by using ESD withstand voltage data from the human body model (HBM) as a reference for workers (human bodies), and ESD withstand voltage data from the charged device model as a reference for devices and jigs.

4.2.2.3 Basic Electrostatic Discharge Controls\textsuperscript{23), 24)}

(1) Countermeasures for the human body

Workers who directly handle semiconductor devices or boards on which devices have been mounted should wear both wrist straps and ESD protective shoes. The charge potential of the human body varies greatly according to worker movements, and the charge potential may rise sharply due to a motion such as standing up from a chair. (Fig. 4-10) Always use a wrist strap with a cord. If the wrist strap is not used in the condition with the body and the ground constantly connected by the cord, the human body cannot be maintained at a stable low potential. Note that the cord may be severed if a sudden load is placed on the cord during the work.

Be sure to use the wrist strap adhered closely to bare skin. If the wrist strap is worn over clothing, the necessary resistance value between the human body and the ground cannot be secured.

If the soles of ESD protective shoes become dirty, the contact resistance between the human body and the floor increases and the prescribed leak resistance may not be obtained. Also, if a worker sitting in a chair places both feet on a footrest or other pedestal, conductivity between the floor and the human body is not obtained and the constantly required electrostatic leakage effects cannot necessarily be maintained. Therefore, safety can be most effectively assured by having workers who directly handle devices wear both wrist straps and ESD protective shoes.

Gloves and finger sacks with ESD protection should be used. In particular, the finger sacks used when handling devices with bare hands must be conductive or electrostatic diffusive. If the surface of finger sacks becomes charged, an electrostatic charge is induced in the device when a device is held, and the risk of the charged device model (CDM) discharge phenomenon occurring increases. (Figs. 4-11 and 4-12)
(a) Measurement method

(b) Measurement results

Fig. 4-10 Changes in the Charge Potential of the Human Body

Fig. 4-11 Human Body (Worker) Countermeasures

Fig. 4-12 Wrist Strap Usage
(2) Work surface

Work surfaces should be covered with ESD protective sheets (made from conductive materials or materials having electrostatic dissipative characteristics) or work tables should be made from materials having these same characteristics. Also, work surfaces must be grounded. (Fig. 4-13) Insulated objects that easily generate static electricity should not be placed on work surfaces. Fixtures and jigs required for work should be made from conductive or electrostatic diffusive materials, and when that is not possible, ionizers should be used. The use of insulated objects for items that may contact or approach devices should be avoided as much as possible, especially during work. Also avoid working with insulated sheets or plates on worktables. The seat and backrest surfaces of chairs that workers sit in should have ESD protective covers, or ESD protective chairs should be used. (Fig. 4-14) Static electricity with an extremely high potential may be generated momentarily when standing up from a chair. (Fig. 4-10)

Fig. 4-13 Work Surface

Fig. 4-14 Chair

(3) Floor

Floors in the work area should be ESD protective floors or covered with ESD protective sheets. When the entire work area floor cannot be covered, at the very least lay ESD protective sheets in the work area where workers wearing ESD protective shoes handle devices or boards on which devices have been mounted. When laying ESD protective sheets, be sure to ground all of the sheets. (Fig. 4-13)

(4) Equipment and facilities

The frames of equipment such as mounters, solder baths and measuring instruments, and facilities for conveying must be grounded. Metal parts that are isolated from the grounded frame by insulating material and that may contact devices should be grounded individually. Insulating material parts that may contact or approach devices should be changed to materials with electrostatic dissipative characteristics, or charges should be eliminated using ionizers.
Both the body and tips of electric screwdrivers, soldering irons and other tools should be grounded. Otherwise, electric over stress (EOS) breakdown may occur if there is an AC voltage leak.

(5) Environment

It is generally considered difficult for static electricity to occur at higher humidity (moisture density in the air). However, what actually happens is that static electricity may be generated but the proportion of the generated charge that leaks due to moisture adhered to the surface increases, so charging appears difficult to occur as a result. In process humidity control it is important to maintain a humidity environment that makes it difficult for static electricity to occur. In actual processes, however, heat generation by equipment and other factors create spaces with locally high temperatures (low relative humidity).

Furthermore, boards that generate heat when the power is on, components packed in plastic trays and bags, and products stored for long periods inside dry warehouses may not necessarily always be in a condition that inhibits the generation of static electricity. Therefore, it is extremely dangerous to think that static electricity can be uniformly inhibited by increasing the humidity, or that other electrostatic discharge control can be omitted. Humidity environment control must be understood only as an auxiliary electrostatic control.

(6) Storage and transport

Semiconductor devices should be stored in the packing format for shipment. Correctly storing devices in the same ESD protective packing materials as when shipped reduces the risk of electrostatic breakdown even when devices are handled during storage.

In addition, boards on which devices are mounted must be stored in containers or on storage shelves made from conductive or electrostatic dissipative material. (Figs. 4-15 and 4-16) At this time, the use of insulated partitions or storage in insulated bags should be avoided. Mounting boards are made from insulating materials, so boards may become charged by vibration or rubbing during storage or transport. In addition, if they are placed near charged objects, an inductive charge may be generated in the board wiring pattern, and may discharge from the connectors during measurement or assembly and damage the device.
(7) Mounted or assembled components other than devices

Many components other than semiconductor devices that are mounted on boards become electrostatically charged during board mounting. Mounted components such as capacitors, filters, LCD panels and flexible connectors that consist of metal and insulating material and have capacitances capable of accumulating static electricity may cause ESD during board mounting and damage devices.

Parts boxes used to store these components and delivery packing must have electrostatic countermeasures. (Fig. 4-17) Workers should be aware that some mounted components other than devices can also carry electrostatic charges, and countermeasures must be taken to prevent these components from causing ESD during board mounting.

(8) Module and set components

Optical pickups, camera modules and other module products that include semiconductor devices may experience ESD breakdown when handled in module units. Even after semiconductor devices are mounted in a module, when device pins are directly exposed to the outside via connectors, the module should be handled in the same manner as the device unit.

Within the set assembly process, metal chassis, cables and other components that consist of metal and
insulating materials, and already assembled components such as display LCD panels, optical disc drives, optical pickups and various modules may carry charges that are discharged to mounting boards via connectors during set assembly, resulting in damage to semiconductor devices. Thorough care should also be taken for charges carried by set components during set assembly.

(9) Eliminating charges using an ionizer

Ionizers are charge elimination equipment that generate corona discharge by applying a high voltage to the tip of a discharge electrode, and neutralize static electricity with the generated ions. Ionizers are an effective means of eliminating static electricity from insulating material that cannot be discharged by grounding. Unlike charges on metal, there is no risk of charges on insulating material being discharged to and damaging devices. However, these charges may generate inductive charges in devices and metal parts. Ionizers are effective when using insulating material near devices.

(10) Clothing

Workers should make efforts to wear clothing made from materials that do not generate static electricity. Clothing made from materials that easily generate static electricity may induce strong static electricity in human bodies with movement.

(11) Characteristics required of ESD protective items

The values given in the table below are references for the characteristics required of main ESD protective items. Even when the characteristics noted in the Specifications satisfy the required standards, the actual effects of countermeasures should be thoroughly verified without fail before selecting ESD protective items for introduction.

<table>
<thead>
<tr>
<th>ESD protective item</th>
<th>Range of resistance values</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floor</td>
<td>Rg≤1×10^9Ω</td>
<td></td>
</tr>
<tr>
<td>ESD protective sheet (Floor, work surface, storage rack)</td>
<td>Resistance between two points</td>
<td>R≤1×10^9Ω</td>
</tr>
<tr>
<td></td>
<td>Resistance between EPA and ground</td>
<td>R≤1×10^9Ω</td>
</tr>
<tr>
<td>ESD protective shoes (when worn on the metal plate)</td>
<td>Resistance between EPA and ground</td>
<td>1×10^5≤R≤1×10^6Ω</td>
</tr>
<tr>
<td>Wrist strap (band)</td>
<td>Resistance value</td>
<td>R≤1×10^6Ω</td>
</tr>
<tr>
<td>Wrist strap (cord)</td>
<td>Resistance value between pins</td>
<td>R≤5×10^5Ω</td>
</tr>
<tr>
<td>Wrist strap (when worn)</td>
<td>Resistance between EPA and ground</td>
<td>R≤3.5×10^6Ω</td>
</tr>
<tr>
<td>Chair</td>
<td>Resistance between EPA and ground</td>
<td>R≤1×10^10Ω</td>
</tr>
<tr>
<td>Clothes</td>
<td>Resistance between two points</td>
<td>R≤1×10^12Ω</td>
</tr>
</tbody>
</table>

Note 1) EPA: ESD Protected Area
<References>
3) JEITA EIAJ ED-4701/304, JEITA (2001)
6) EIA/JESD 22-A115E, JEDEC, (2008)
8) JESD22-C101E, JEDEC, (2008)
20) Tanaka et al., “Electrostatic Breakdown Phenomenon in LSI due to Displacement Current”, RCJ 6th EOS/ESD


4.2.3 EMC (Electromagnetic Compatibility)

Semiconductor devices and system circuits may misoperate or functions may be impaired according to the ambient electromagnetic environment. This is because in addition to the effects from external equipment, noise generated from high-speed switching power supply circuits, digital circuits and printed wiring boards is emitted and conducted via various paths, and affects semiconductor device and system circuit operation. Recent increases in mounting density, higher frequencies, and expansion of analog-digital mixed systems are further complicating this situation.

To address these problems, it is important to determine noise sources and understand transmission paths. Appropriate measures must be taken to prevent problems such as reinforcement of GND, optimization of circuit layout patterns, and application of electromagnetic shielding and electromagnetic wave absorbers to semiconductor devices and set circuits.

4.2.4 Strong Electric and Magnetic Fields

Strong external electromagnetic fields are generally not the direct cause of device failure. However, when devices are exposed to strong magnetic fields, the impedance may change, the leak current may increase, or other abnormal phenomena may occur due to polarization of the package plastic materials or inside the IC chip.

In addition, if power supplies or parts that generate high voltages are located near devices, large noise in the power supply or ground lines may cause circuits to misoperate or the IC to generate noise.

To prevent these external electromagnetic interferences from impeding circuit functions, circuit layout patterns and component arrangements on printed boards are optimized and shielded wires are used. In addition, care must be given to the set design, such as changing mounting locations or providing electric and/or magnetic field shielding as necessary.

4.2.5 Overvoltage Breakdown (EOS Breakdown)

Failure modes where overvoltage or overcurrent other than static electricity causes breakdown are called overvoltage breakdown or electric over stress (EOS) breakdown. Electric over stress has various causes, but device burnout failure is generally caused by the application of pulse-type electric over stress called surge. Causes of surge include discharge from capacitive loads due to equipment power-on/off or relay switching, and lightning surge due to lightning strikes, etc.

The surge-induced EOS breakdown mechanism varies according to the type of applied surge, but applying voltage in excess of the ratings to the device power supply or input/output pins causes junction breakdown inside the device or the phenomenon where parasitic transistors are activated. At this time, if an overcurrent flows and the energy consumed by the metal wiring and transistors exceeds the wiring or junction endurance level, the wiring may melt or junctions may suffer thermal breakdown.
Countermeasures against EOS breakdown include inserting voltage clamp diodes or capacitors to the power supply and input/output pins on the board to prevent surges from entering the inside of the board. This requires noise countermeasures for measuring instruments used to adjust boards within processes.

4.2.6 Handling of High-frequency Devices

As semiconductor devices incorporate more advanced functions and performance, the device structures are being further miniaturized with higher densities, and oxide films and wiring layers are becoming thinner. This has resulted in an intrinsic drop in electrostatic strength.

To increase the electrostatic strength, countermeasures such as adding electrostatic protection circuits to device input/output pins are generally taken, but this also has the drawback of causing characteristics degradation.

Particularly for high-frequency and high-speed devices, adequate electrostatic countermeasures cannot be taken for some pins in order to satisfy the required performance. For example, since electrostatic protection elements with adequate electrostatic strength and low capacitance are necessary for input/output pins of high-speed transmission interface devices such as LVDSs, MIPIs, measures against ESD for which both performance and strength are essential have become a problem.

Therefore, thorough countermeasures must be taken in all aspects from device storage and transport to set mounting, inspection and other work environments, and also for handling during work.

4.2.7 Latch-up

Latch-up is the phenomenon where overvoltage or current stress such as static electricity or noise entering from an external source triggers the parasitic thyristors in CMOS devices and creates a short-circuit between the power supply and GND.

The latch-up phenomenon occurs in the operating condition (the condition with the supply voltage applied), but as long as voltage stress that exceeds the device ratings is not applied, there is little or no risk of latch-up occurring within the normal operating voltage range. Latch-up that occurs randomly while using electronic equipment is thought to be mostly caused by the entry of stress in excess of the ratings to products incorporating semiconductors or the occurrence of this type of situation during operation. Possible causes of latch-up are as follows.

(1) Entry of static electricity from an external source

When static electricity enters an operating device that is mounted on a board, the discharge current passes through the input/output pin protective elements and flows to the power supply or GND wiring. In consideration of discharge from human bodies, the peak current value that flows at an ESD of several kV can reach several A to several ten A. If this current flows to the board power supply or GND wiring, the power supply or GND potential fluctuation may reach several V and exceed the device ratings. If this voltage fluctuation occurs during device operation, the junctions inside the device may break down and cause latch-up.
Portable electronic equipment (cellular phones, camcorders, laptop computers, portable data terminals, digital cameras, etc.) has spread rapidly in recent years, and the frames of this electronic equipment that is frequently and directly touched by people is not grounded. Therefore, this equipment is easily affected by supply voltage fluctuations caused by ESD from human bodies, and has a high risk of latch-up.

(2) Entry of lightning surge

Semiconductor devices used in communications facility or power supply facility equipment may experience latch-up due to lightning surge entering via communication cables or transmission lines. Household electronic products may also experience latch-up due to lightning surge entering through utility poles, transmission cables or telephone lines, etc.

(3) Electromagnetic susceptibility (EMS)

If sources of electromagnetic noise (car engines, cathode ray tubes, ESD) are present around electronic equipment, noise induced by sudden changes in the electromagnetic field may cause latch-up.

(4) Live wire insertion or removal

When performing maintenance or repair work on operating systems, depending on the manner in which the connectors are connected, voltage may be applied to the input/output pins before power is supplied to the board when a board is inserted with the system in the operating condition. At this time, the input/output pin potential momentarily becomes higher than the supply voltage, causing an influx of current from the pin and resulting in latch-up.

(5) Supply voltage application sequence for multi-power supply devices

In devices with multiple different power supplies, the potential of certain pins may rise above the supply voltage depending on the sequence in which the supply voltages are applied, and this may cause latch-up. Care must be taken for the order in which the power supplies are applied to the device for devices that use multiple power supplies.

Latch-up caused by these types of external factors can be suppressed by taking countermeasures to prevent the entry of surges and noise that serve as the respective triggers. Effective countermeasures for static electricity or surges that directly enter pins include inserting surge countermeasure diodes, capacitors or other elements to the board entrances that are the entry routes, or using board power supply and GND wiring patterns that are resistant to potential fluctuations and noise. In addition, lowering the power supply and GND wiring impedance, suppressing potential fluctuations due to sudden currents, and separating the power supply and GND wiring of circuit blocks that are susceptible to external surges from other circuits are also effective countermeasures. Countermeasures for the power supply application order include inserting capacitors or taking other measures to delay the respective rise timings, etc.

Electromagnetic noise requires shielding countermeasures to prevent electromagnetic waves from entering...
electronic equipment or the use of wiring patterns that are resistant to induction by electromagnetic fields. When sources of electromagnetic noise are present inside equipment, countermeasures must be taken for the noise source or the power supply and GND wiring must be separated, etc.

4.2.8 Thermal Runaway

Thermal runaway is the phenomenon where positive feedback increases the power due to the temperature characteristics of the IC internal circuits, causing the temperature to rise without limit and resulting in failure. Most failure after mounting is thought to be caused by thermal runaway. In addition to thermal runaway caused by local heat generation in the device, thermal runaway may also occur depending on the heat radiation structure in power devices. Therefore, special care must be given to heat radiation design.
4.3 Notes on Handling for Mechanical Breakdown

Devices should be handled carefully. Devices may be damaged by dropping or shocks, so care should be taken to keep mechanical vibrations and shocks to a minimum.

Devices are comprised of chips, bonding wires, external pins, radiation fins, mold resin and other elements, and the mechanical strength and coefficient of thermal expansion of each component material differ. Therefore, mechanical breakdown may occur in various cases such as when forming or cutting external pins, mounting devices on printed boards, washing, or attaching radiation fins.

These mechanical external forces may cause package or chip cracking, and lead to degraded moisture resistance due to delamination at the boundary between the mold resin and the external pins.

4.3.1 Forming and Cutting External Leads

When mounting semiconductor devices onto printed boards, care should be taken not to apply excessive force to the external leads when forming or cutting the external leads beforehand. (Fig. 4-18)

![Fig. 4-18 Notes on Forming or Cutting External Leads](image)

(1) When bending external leads, clamp the external lead between the point at which the lead is to be bent and the package body. Do not bend external leads while holding the package body.

When using a metal mold, also do not apply stress to the package body.

Likewise, when cutting external leads, do not apply stress to the package body.

(2) Do not repeatedly bend external leads.

(3) Do not bend external leads in the thick direction of the lead.

(4) Care should be taken as the external lead plating may be damaged depending on the bending method.

4.3.2 Mounting Devices on Printed Boards

When mounting semiconductor devices on printed boards, care must be taken not to apply excessive stress to the external leads. If the external leads bend or float, good solder contact with the printed board may not be obtained, resulting in a mounting defect. (Fig. 4-19)
(1) The external lead attachment interval on the printed board should match the external lead interval of the device.

(2) When inserting the device into the printed board, avoid forcibly inserting the device.

(3) Leave an appropriate gap between the semiconductor device and the printed board.

(4) When mounting a surface mounted-type device on a printed board, if the external leads are deformed or float, good solder contact with the printed board may not be obtained, resulting in a mounting defect. Therefore, care must be taken not to deform the external leads.

(5) When mounting semiconductor devices on printed boards using mounting sockets, use an appropriate socket for each package.

Correct Incorrect

Semiconductor Device

Mounting does not apply stress to the lead base (arrows).

The leads were forced into the lead holes of the printed board, so stress is needlessly applied as indicated by the arrows.

Fig. 4-19 Notes on Printed Board Mounting

4.3.3 Washing Methods

In principle, flux must be removed after soldering. Otherwise, flux residue may affect the reliability of components, printed board wiring or solder junctions.

(1) Ultrasonic washing offers excellent washing effects in a short time, but the following care must be given in order to prevent device breakdown:

① Determine proper frequency applied, output, and washing time.

② Avoid direct contact with the device and another device, the printed board and/or the main frame of the ultrasonic washers.

(2) Do not rub marked surfaces during washing or while detergent has adhered to the device, as this may cause the marking to disappear.

Care should also be taken as the marking may disappear if washing is performed for a long time.

(3) Even when using solvents or washing just with water, washing should be performed so that sodium, chlorine and other reactive ions do not remain. Also, be sure to dry all parts thoroughly.

(4) When using solvents, be sure to take into account public environmental standards and safety standards.
4.3.4 Attaching Radiation Fins

Care should be taken for the following points when attaching radiation fins to devices.

(1) Use an appropriate attachment method so that excessive stress is not applied to the device.

(2) Take care for flatness so that there is no burring or unevenness on radiator fins.
   
   If radiator fins are inappropriate, sufficient radiation effects may not be obtained, and forced attachment may cause device characteristics degradation or mechanical breakdown.

(3) When there are two or more radiator fin mounts, first lightly pre-tighten all of the mounts, then tighten to the prescribed torque.

(4) Do not attach radiator fins to a semiconductor device after the device has been mounted on a board.
   
   Otherwise, excessive stress may be applied to the semiconductor device depending on the manner in which the device is mounted on the board. First attach the radiator fins to the semiconductor device, and then mount the device on the board.

(5) Thermal conductivity is generally improved by coating the junction between radiator fins and semiconductor devices with silicon grease. In this case, be sure to apply an even coat.
4.4 Notes on Handling to Prevent Thermal Breakdown

Semiconductor devices have structures that combine a silicon chip, plastic encapsulating materials, copper and other metallic lead frames, and other materials, each of which has completely different thermal properties. In particular, when the plastic materials are exposed to high temperatures such as during soldering, the moisture accumulated in the plastic rapidly turns into steam and causes package cracking. The causes of delamination between the adhered portions of component materials, disconnection of conductors and other problems brought about by repeated heat stress are as follows.

1. The mechanical strength drops significantly at high temperatures.
2. Moisture in the air is absorbed and accumulated.

This section describes general precautions, particularly for product mounting, to prevent this type of thermal breakdown of devices.

4.4.1 Soldering

(1) Precautions during soldering

Semiconductor devices generally should not be left for long periods at high temperatures.

Even during soldering, regardless of whether hand soldering or reflow methods are used, if the soldering temperature is high and the soldering time is long, the device temperature may rise and result in degradation or breakdown. Therefore, soldering should be performed at the lowest temperature and shortest time possible.

(2) When soldering through-hole device (THD) packages with a wave solder vat

This method dips the portions of the package lead pins to be soldered into the liquid surface of a jet solder bath. However, note the package may be damaged if the jet solder contacts the package body, so care should be taken not to allow the solder to directly contact the package body.

In addition, when using a wave solder bath, the bottom of the board is heated by the solder heat, so board warping may occur due to the temperature difference between the top and bottom of the board.

If soldering is performed with the board in the warped condition, the board attempts to return to its original condition when it is taken from the solder bath, so excessive stress may be applied to the leads and package, causing solder junction cracking and lead and package damage.

Therefore, when using a wave solder bath, soldering should be performed in a manner that does not produce board warping.

4.4.2 Notes on Mounting Surface Mount Devices (SMD)

Board mounting methods for SMD include infrared reflow, air reflow, and vapor phase reflow, etc. Thus, soldering methods that heat the entire package are often used.
In contrast to conventional THD where only the external lead pins are heated, the entire SMD package is suddenly exposed to high temperatures, so mold resin cracking and degraded moisture resistance must be taken into account as potential reliability problems.

In addition, SMD have short external lead pins, narrow pin intervals and large numbers of pins to facilitate high-density mounting. Therefore, sufficient care must be taken when handling SMD.

General precautions when mounting SMD products are described below.

(1) **Notes during mounting**

When soldering is performed by infrared reflow or other methods that heat the entire device in the condition where the mold resin has absorbed moisture due to long-term storage in the normal environment or storage in a high-humidity environment, the mold resin may crack or delamination may occur at the chip boundary.

See section “4.1.3 Notes on Package Cracking” for points during mounting.

(2) **Deformation of external lead pins**

If the external lead pins bend or float, good solder connection with the board may not be obtained, resulting in mounting defects. Particular care must be taken for the flatness of external leads so that pins do not float during mounting.

In addition, when mounting SMD, if strict control is performed for only the external lead pins and the board control is insufficient, good solder connection may not be obtained. Full care should be given to board warping and cream solder film thickness and uniformity, etc.

(3) **Handling of taping parts**

When using taping-packed SMD, static electricity is generated when the top cover tape is peeled from the carrier tape, and the SMD may become charged. This charge voltage increases as the speed at which the top cover tape is peeled becomes faster. High-speed tape peeling and rubbing should be avoided as much as possible to prevent electrostatic breakdown.

(4) **Other precautions**

When coating SMD and other devices with plastic after mounting on a board, moisture absorption may cause the leak current to increase depending on the coating plastic, or the stress of the coating plastic may also produce mechanical stress on the plastic portions of devices. Therefore, post-coating reliability must be thoroughly confirmed when selecting the coating materials.
4.5 Notes on Product Specifications, Packing, Transport and Storage

4.5.1 Product Specifications

4.5.1.1 Notes on the Use of Semiconductor Devices

Sony makes the utmost efforts to improve quality and reliability, but due to the nature of semiconductor devices, a certain percentage of devices may malfunction or fail. When using semiconductor products manufactured by the Sony Semiconductor Business Unit, customers are requested and responsible for ensuring safe equipment and system designs to prevent accidents resulting in death, injury or damage to property from occurring as a result of semiconductor failure.

Note that when designing equipment and systems, the latest product specifications should be checked, and products should be used within the assured ranges.

Semiconductor products listed in catalogs and sold assume use in general electronic equipment (home appliances, telecommunications equipment, measuring instruments, office equipment, etc.). Customers should be sure to consult their Sony sales representative beforehand when planning use for applications requiring special quality and reliability, or in equipment and systems (automobiles, traffic equipment, medical equipment including life-support devices, safety devices, aerospace equipment, nuclear power control equipment, etc.) where product failure or malfunction may pose a direct life- or injury-threatening risk or damage to property. Special consideration and selection is required for products that demand high reliability.

4.5.1.2 Maximum Ratings (Absolute Maximum Ratings)

The maximum ratings of semiconductor devices are normally prescribed by the [Absolute Maximum Ratings]. According to JIS C 7032, absolute maximum ratings are prescribed as “Limit values which must not be exceeded even momentarily, or limit values for which the values of two or more items must not be reached simultaneously when specification values are established for two or more items.” Exceeding absolute maximum ratings even temporarily causes degradation or failure, and even if the product continues to operate for some time thereafter, the life is significantly shortened.

Therefore, when designing electronic circuits using semiconductor devices, care must be taken not to exceed the maximum ratings of these devices even due to fluctuations caused by external conditions during operation.

Maximum ratings indicate the operating limit values for that IC, and parameters such as those shown in Table 4-7 are generally prescribed. When actually using ICs, operation must stay within these prescribed ranges.
<table>
<thead>
<tr>
<th>Item</th>
<th>Conditions</th>
<th>Rating value</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (V_{DD}) (V_{CC})</td>
<td>Ta=25°C Measured relative to the VSS pin</td>
<td>7.0V</td>
<td>This is the maximum voltage that can be applied between the power supply pins and the GND pins.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(for a 5.0 V device)</td>
<td>1. This is related to the endurance voltage of the transistors inside the IC, and breakdown may occur if this voltage is exceeded.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. CMOS devices may break down due to latchup or the injection of large quantities of hot carriers.</td>
</tr>
<tr>
<td>Input and output voltages (V_{IN}) (V_{OUT})</td>
<td>Ta=25°C Measured relative to the VSS pin</td>
<td>-1.0 to 7.0V</td>
<td>This is the maximum voltage that can be applied between the input/output pins and the GND pins.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1. This voltage generally cannot be larger than the supply voltage.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Parasitic elements configured on the input and output pins may experience endurance voltage-related breakdown.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. Breakdown may be caused by latch-up triggered by the input or output pins.</td>
</tr>
<tr>
<td>Allowable power dissipation (P_{D})</td>
<td>Ta=25°C</td>
<td>1W</td>
<td>This is the maximum power consumption allowed inside the IC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1. Breakdown may be caused by internal heat generation during operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2. This value differs according to the degree of IC integration and the heat radiation characteristics of the package.</td>
</tr>
<tr>
<td>Storage temperature (T_{stg})</td>
<td></td>
<td>-55 to 150°C</td>
<td>This is the allowable ambient temperature range during storage.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1. The temperature is limited by the package materials and the intrinsic properties of semiconductors.</td>
</tr>
<tr>
<td>Junction temperature (T_{j})</td>
<td></td>
<td></td>
<td>This is the maximum allowable junction temperature value at which continuous operation is possible.</td>
</tr>
<tr>
<td>Operating temperature (T_{opr})</td>
<td></td>
<td>-10 to 70°C</td>
<td>Recommended operating temperature condition range. IC operation and functions can be assured within this temperature range, but the electrical characteristics indicated at Ta = 25°C cannot necessarily be assured.</td>
</tr>
</tbody>
</table>

Note) Rating values are prescribed by the individual specifications for each device.
Fig. 4-20 shows the relationship between various IC maximum ratings.

![Fig. 4-20 Relationship between Various Maximum Ratings](image)

### 4.5.1.3 Operation Assurance Range

The operation assurance range indicates operating conditions that must be observed to realize the operations and functions noted in the data book. Even when the maximum ratings are not exceeded, use outside the operation assurance range may impair device operations and functions, prevent electrical specifications from being satisfied, or lead to reduced reliability, so sufficient care should be taken for the system design.

In addition, to ensure reliability when using devices, perform derating with respect to the current, power and temperature of the operation assurance range.

### 4.5.1.4 Derating

Derating refers to preventing drops in device reliability by setting operating conditions that are less than the various rating values of a device, and taking into account power supplies, surge and noise to input pins, and other factors.

Derating is generally performed with respect to electrical stress such as voltage, current and power, and environmental stress such as ambient temperature and humidity. Power devices in particular generate large amounts of heat, so sufficient care should be taken as reliability varies greatly due to the degree of junction temperature (Tj) derating.
4.5.2 Notes on Packing, Transport and Storage

Semiconductor devices (hereafter “devices”) maintain high quality and high reliability, but improper handling, transport, storage or use may lead to device breakdown or deterioration. Causes of device breakdown include electrostatic breakdown during handling, package cracking during mounting due to package moisture absorption, and mechanical breakdown due to shocks and lead bending. Items that should be kept in mind are described below.

4.5.2.1 Notes on Packing

The following three storage case packing formats are mainly used in accordance with the device package shape and mounting format.

(1) Tray  (2) Magazine  (3) Embossed taping

The packing materials used by these packing formats should use structures and materials suited to each device to maintain device quality.

Notes on each packing format are described below.

(1) Tray packing

Trays come in heat-resistant specifications and normal temperature specifications. Heat-resistant specification trays are marked “HEAT PROOF” or indicate the heat resistance temperature such as “135°C MAX”. When devices are to be baked (dried at high temperature), observe the device baking conditions and perform baking within the heat resistance temperature range of the tray (125°C MAX for trays marked with “HEAT PROOF”).

Baking cannot be performed using normal temperature specification trays, so when devices in normal temperature specification trays are to be baked, these devices must be transferred to heat-resistant specification trays. Anti-static measures should be taken to prevent ESD breakdown before transferring devices from a tray. Also, be careful not to bump or press the electrode pins against the tray to prevent electrode pin deformation.

Fig. 4-21 Tray

(2) Magazine packing

Magazine surfaces are coated with a water-soluble anti-charging agent. Therefore, note that the anti-charging effects will be lost if the magazine is dampened by water or stored in a high-temperature and high-humidity location, or if devices are allowed to slide back and forth.

In addition, magazines do not have heat-resistant specifications, so when devices are to be baked, transfer the devices to a metal magazine or other heat-resistant storage case. At this time, care should be taken to prevent
lead bending, and anti-static measures should be taken to prevent ESD breakdown.

![Fig. 4-22 Conductive Magazines](image)

**Fig. 4-22 Conductive Magazines**

**3) Embossed taping packing**

Taping does not have heat-resistant specifications, so when devices are to be baked, transfer the devices to a heat-resistant storage case.

When transferring the devices, care should be taken to prevent electrode pin deformation and ESD breakdown.

In addition, the taping peeling strength is affected by the temperature and humidity of the storage environment, so care should be taken when setting a tape reel in a mounter.

The peeling strength measurement method conforms to JIS C 0806-3:1999.

![Fig. 4-23 Taping](image)

**Fig. 4-23 Taping**

**4.5.2.2 Notes on Transport**

Devices contained in trays, magazines and embossed taping are stored and shipped in our specified packing cartons to avoid the effects of external shocks during transport, rain water during storage, or contamination from the outside air, etc.

If handling is rough and strong shocks are applied during transport, devices may experience lead bending or other damage, resulting in trouble during mounting.

In addition, rough handling may also cause the aluminum laminate bags used as moisture-proof packing to become torn. If the aluminum laminate bags become torn, the devices may absorb moisture, resulting in problems that affect device quality.

Therefore, care should be taken for the following points during transport.

1. Efforts are made to minimize shocks, vibration, humidity and other adverse effects applied to devices. However, application of excessive shocks or vibration may damage devices, so care should be taken for handling to reduce shocks and mechanical vibration.

2. Avoid exposure to direct sunlight and take care to prevent condensation.
(3) If packing boxes are received in a damaged condition, do not open the packing boxes, and contact your Sony sales representative.

(4) Care marks indicating cautions are displayed on packing boxes as necessary. Be sure to follow these instructions for storage and transport. Examples of care mark indications are shown below.

- **Fragile**
  If packing cartons are thrown or dropped during handling, the packing materials and possibly the devices themselves may be damaged. Handle packing cartons with care.

- **This side up**
  Packing cartons should be placed facing the correct direction as indicated on the packing carton during transport. If packing cartons are turned upside down or on their sides, unnatural force may be applied to and damage devices.

- **Keep dry**
  When cartons absorb water, the strength drops drastically, so cartons must not be allowed to become wet, especially during transport in rain or snow.

- **Avoid static charges**
  This is not a caution during transport, but is indicated as a caution during set mounting.

### 4.5.2.3 Notes on Storage

The storage environment affects quality, so control the following items when storing devices.

1. **Storage environment**
   Store indoors under ambient conditions of normal temperature and humidity [temperature (5°C to 35°C), humidity (30% to 75%)].

2. **Storage period**
   The storage limits for each packing format in the above storage environment are as follows.
   - Products in tray packing: 1 year from delivery date
   - Products in magazine packing: 1 year from delivery date
   - Products in taping packing: 1 year from delivery date
The storage limit for each packing format is 1 year. Exceeding this limit may result in reduced device solderability, deteriorated water-soluble anti-charging agent effects, unstable peeling strength of taping packed products, or other problems.

(3) Atmosphere

Avoid storage in locations exposed to direct sunlight, locations where corrosive gases are generated, or dusty locations.
- Storing cases (magazines or non-heat-resistant trays) may deform if exposed to direct sunlight.
- Corrosive gases cause the external lead pins of devices to corrode and solderability to deteriorate.

(4) Temperature changes

Moisture condenses on packed products in locations where the temperature changes suddenly. To avoid condensation, store semiconductor devices in locations where the temperature changes as little as possible.

(5) Avoid stacking or placing heavy objects on packing boxes as much as possible to avoid applying loads to devices.

(6) Store devices in locations not exposed to radiation, strong electromagnetic fields or static electricity.

(7) When storing devices for long periods, different moisture-proof packing and packing components must be used.

Devices stored for long periods may experience deteriorated pin solderability, rust, or electrical characteristic failure. Contact your Sony sales representative beforehand when long-term storage is anticipated.

(8) Products in moisture-proof packing

Moisture absorption affects device quality, and moisture-proof packing aims to prevent moisture absorption during storage. Devices, desiccants and moisture indicators are placed in aluminum laminate bags that are deaerated and heat-sealed to block outside air and prevent the entry of moisture.

If moisture enters the moisture-proof packing, the devices may absorb moisture. Exposing devices that have absorbed moisture to high-temperature ambient conditions such as the soldering process during mounting may result in package cracking or other quality problems. Moisture-proof packing is used to prevent these kinds of effects on quality.

Devices begin to absorb moisture as soon as the moisture-proof packing is opened, so control should be performed so that devices are used within the specified time in accordance with the SMD rank instructions.

When the period specified by the SMD rank is exceeded, baking must be performed again. Contact your Sony sales representative for the baking time for each device.

In addition, moisture indicators are enclosed as simple indicators of the humidity condition inside moisture-
proof packing. When the indicated humidity immediately after opening the moisture-proof packing exceeds 30%, some trouble may have occurred, so contact your Sony sales representative.

Fig. 4-25 Moisture-proof Packing