[Product Information]

Ver.1.3

IMX422LLJ

Diagonal 9.2 mm (Type 1 / 1.7) CMOS solid-state Image Sensor with Square Pixel for
Monochrome Cameras

Description

The IMX422LLJ is a diagonal 9.2 mm (Type 1 / 1.7) CMOS active pixel type solid-state image sensor with a square
pixel array and 2.03 M effective pixels. This chip features a global shutter with variable charge-integration time. This
chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption.
High sensitivity, low dark current and low PLS characteristics are achieved.
(Applications: FA cameras, ITS cameras)

Features

◆ CMOS active pixel type dots
◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
◆ Global shutter function
◆ Input frequency
  37.125 MHz / 74.25 MHz / 54 MHz
◆ Number of recommended recording pixels: 1624 (H) × 1240 (V) approx. 2.01 M pixels
  Readout mode
  All-pixel scan mode
  Vertical / Horizontal 1 / 2 Subsampling mode
  2 × 2 Vertical FD binning mode
  ROI mode
  Vertical / Horizontal - Normal / Inverted readout mode
◆ Readout rate
  Maximum frame rate in
  All-pixel scan mode: 8 bit: 477.6 frame/s, 10 bit: 434.1 frame/s, 12 bit: 270.4 frame/s
◆ 8-bit / 10-bit / 12-bit A/D converter
◆ CDS / PGA function
  0 dB to 24 dB: Analog Gain (0.1 dB step)
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
◆ I/O interface
  SLVS (4 ch / 8 ch switching) output (594 / 297 Mbps per ch)
  SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane switching) output (2.376 / 1.188 Gbps per Lane)
◆ Recommended lens F number: 2.8 or more (Close side)
◆ Recommended exit pupil distance: −100 mm to −∞

Pregius

* Pregius is a trademark of Sony Corporation. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use
Sony’s low-noise CCD structure, and realizes high picture quality.

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**Device Structure**

- **CMOS image sensor**
- **Image size** Diagonal 9.2 mm (Type 1 / 1.7) Approx. 2.03 M pixels All-pixel
- **Total number of pixels** 1632 (H) × 1272 (V) Approx. 2.07 M pixels
- **Number of effective pixels** 1632 (H) × 1248 (V) Approx. 2.03 M pixels
- **Number of active pixels** 1632 (H) × 1248 (V) Approx. 2.03 M pixels
- **Number of recommended recording pixels** 1624 (H) × 1240 (V) Approx. 2.01 M pixels All-pixel
- **Unit cell size** 4.5 µm (H) × 4.5 µm (V)
- **Optical black**
  - Horizontal (H) direction: Front 0 pixel, rear 0 pixel
  - Vertical (V) direction: Front 24 pixels, rear 0 pixel
- **Package** 226 pin LGA

**Image Sensor Characteristics**

(Tj = 60 °C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity (F8)</td>
<td>Typ.</td>
<td>1677 mV</td>
</tr>
<tr>
<td>Saturation signal</td>
<td>Min.</td>
<td>1001 mV</td>
</tr>
</tbody>
</table>

**Basic Drive Mode**

<table>
<thead>
<tr>
<th>Drive mode</th>
<th>Recommended number of recording pixels</th>
<th>Maximum frame rate [frame/s]</th>
<th>Output interface</th>
<th>ADC [bit]</th>
</tr>
</thead>
<tbody>
<tr>
<td>All pixel</td>
<td>1624 (H) × 1240 (V) approx. 2.01 M pixels</td>
<td>239.0 SLVS 8 ch</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>477.6 SLVS – EC 8 Lane</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>194.5 SLVS 8 ch</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>434.1 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>165.4 SLVS 8 ch</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>270.4 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical / Horizontal 1/2 subsampling</td>
<td>812 (H) × 620 (V) approx. 0.50 M pixels</td>
<td>791.5 SLVS 8 ch</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>904.0 SLVS – EC 8 Lane</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>658.5 SLVS 8 ch</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>823.9 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>518.8 SLVS 8 ch</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>518.8 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 × 2 Vertical FD binning</td>
<td>812 (H) × 620 (V) approx. 0.50 M pixels</td>
<td>796.1 SLVS 8 ch</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>909.2 SLVS – EC 8 Lane</td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>662.3 SLVS 8 ch</td>
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<td>12</td>
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<tr>
<td></td>
<td></td>
<td>828.6 SLVS – EC 8 Lane</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>521.8 SLVS 8 ch</td>
<td></td>
<td></td>
</tr>
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<td>521.8 SLVS – EC 8 Lane</td>
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◆ Package 226 pin LGA

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<td>Sensitivity (F5.6)</td>
<td>Typ.</td>
<td>2058 mV 1/30 s accumulation</td>
</tr>
<tr>
<td>Saturation signal</td>
<td>Min.</td>
<td>1001 mV</td>
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<td>SLVS 8 ch, SLVS – EC 8 Lane, SLVS 8 ch, SLVS – EC 8 Lane, SLVS 8 ch, SLVS – EC 8 Lane</td>
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