[Product Information]  
IMX367LLA  
Diagonal 21.6 mm (Type 4 / 3) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

Description

The IMX367LLA is a diagonal 21.6 mm (Type 4 / 3) CMOS active pixel type solid-state image sensor with a square pixel array and 19.66 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, digital 1.2 V, and interface 1.8 V triple power supply, and has low power consumption. High sensitivity, low dark current and low PLS characteristics are achieved. (Applications: FA cameras, ITS cameras)

Features

◆ CMOS active pixel type dots  
◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit  
◆ Global shutter function  
◆ Input frequency  
  37.125 MHz / 74.25 MHz / 54 MHz  
◆ Number of recommended recording pixels: 4416 (H) × 4428 (V) approx. 19.55 M pixels  
  Readout mode  
  All-pixel scan mode  
  Vertical / Horizontal 1 / 2 Subsampling mode  
  2 × 2 Vertical FD binning mode  
  ROI mode  
  Vertical / Horizontal - Normal / Inverted readout mode  
◆ Readout rate  
  Maximum frame rate in  
  All-pixel scan mode: 8 bit: 43.0 frame/s, 10 bit: 39.6 frame/s, 12 bit: 28.3 frame/s  
◆ 8-bit / 10-bit / 12-bit A/D converter  
◆ CDS / PGA function  
  0 dB to 24 dB: Analog Gain (0.1 dB step)  
  24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)  
◆ I/O interface  
  SLVS (2 ch / 4 ch / 8 ch switching) output (594 / 297 Mbps per ch)  
  SLVS - EC (1 Lane / 2 Lane / 4 Lane / 8 Lane) output (2.376 / 1.188 Gbps per Lane)  
◆ Recommended lens F number: 2.8 or more (Close side)  
◆ Recommended exit pupil distance: –100 mm to –∞

Pregius

* Pregius is a trademark of Sony Corporation. The Pregius is global shutter pixel technology for active pixel-type CMOS image sensors that use Sony’s low-noise CCD structure, and realizes high picture quality.

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Device Structure

- **CMOS image sensor**
- **Image size** Diagonal 21.6 mm (Type 4 / 3) Approx. 19.66 M pixels All-pixel
- **Total number of pixels** 4432 (H) × 4446 (V) Approx. 19.70 M pixels
- **Number of effective pixels** 4432 (H) × 4436 (V) Approx. 19.66 M pixels
- **Number of active pixels** 4432 (H) × 4436 (V) Approx. 19.66 M pixels
- **Number of recommended recording pixels** 4416 (H) × 4428 (V) Approx. 19.55 M pixels All-pixel
- **Unit cell size** 3.45 µm (H) × 3.45 µm (V)
- **Optical black** Horizontal (H) direction: Front 0 pixel, rear 0 pixel
  Vertical (V) direction: Front 10 pixels, rear 0 pixel
- **Package** 236 pin PGA

Image Sensor Characteristics (Preliminary)

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity (F8) Typ.</td>
<td>915 mV</td>
<td>1/30 s accumulation</td>
</tr>
<tr>
<td>Saturation signal Min.</td>
<td>1001 mV</td>
<td></td>
</tr>
</tbody>
</table>

(Tj = 60 °C)

Basic Drive Mode

<table>
<thead>
<tr>
<th>Drive mode</th>
<th>Recommended number of recording pixels</th>
<th>Maximum frame rate [frame/s]</th>
<th>Output interface</th>
<th>ADC [bit]</th>
</tr>
</thead>
<tbody>
<tr>
<td>All pixel</td>
<td>4416 (H) × 4428 (V) approx. 19.55 M pixels</td>
<td>28.0 SLVS 8 ch</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>43.0 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>22.7 SLVS 8 ch</td>
<td></td>
<td>10</td>
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<tr>
<td></td>
<td></td>
<td>39.6 SLVS – EC 8 Lane</td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>19.0 SLVS 8 ch</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>28.3 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical / Horizontal 1/2 subsampling</td>
<td>2208 (H) × 2214 (V) approx. 4.89 M pixels</td>
<td>84.2 SLVS 8 ch</td>
<td></td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>84.2 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>77.7 SLVS 8 ch</td>
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<td>10</td>
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<td></td>
<td>77.7 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>55.7 SLVS 8 ch</td>
<td></td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>55.7 SLVS – EC 8 Lane</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 × 2 Vertical FD binning mode</td>
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◆ Readout rate
  - Maximum frame rate in
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<td>1146 mV</td>
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<td>Saturation signal</td>
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